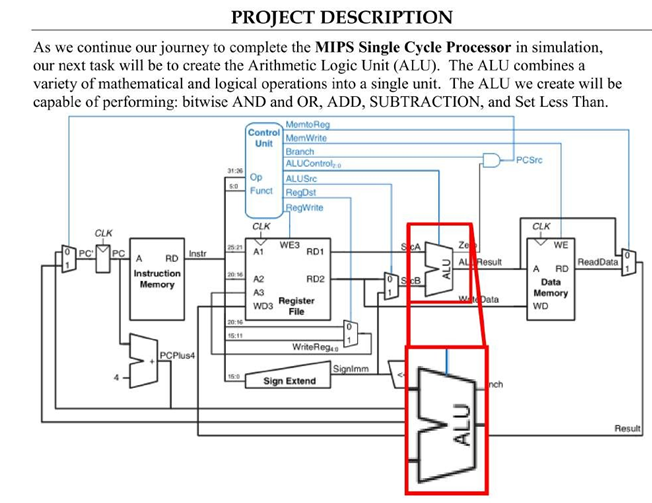
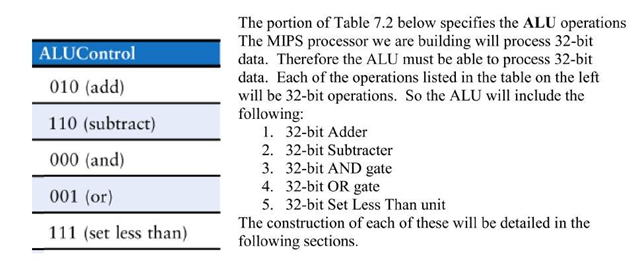
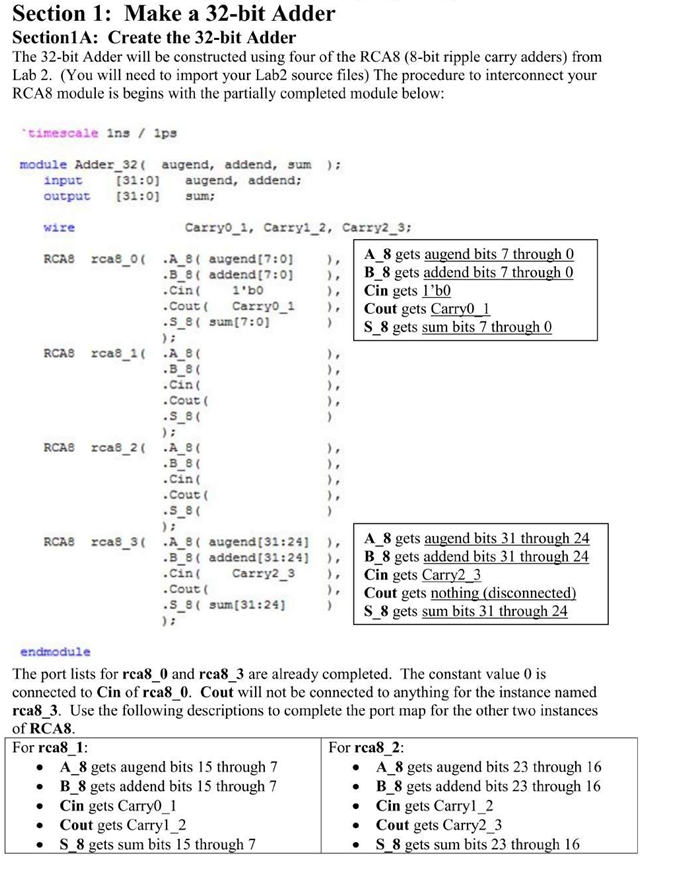
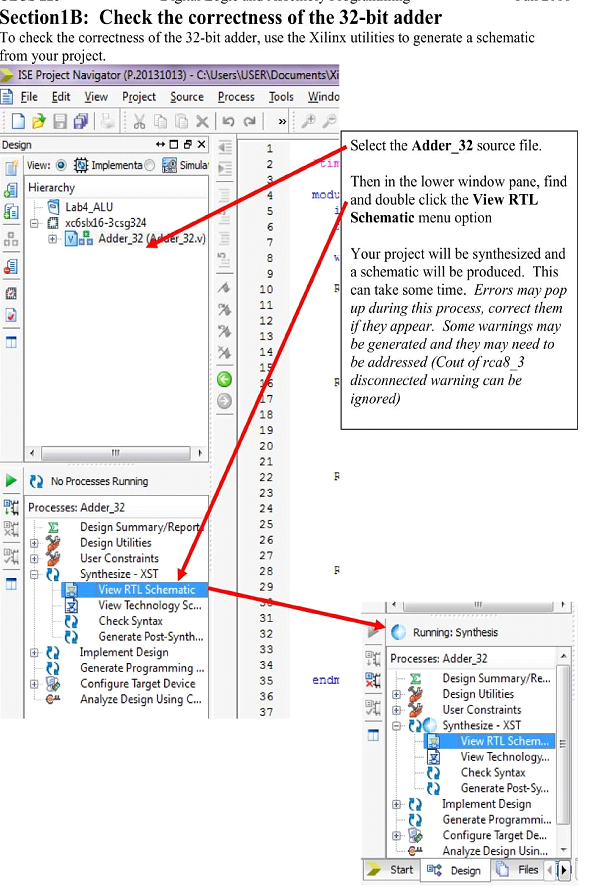
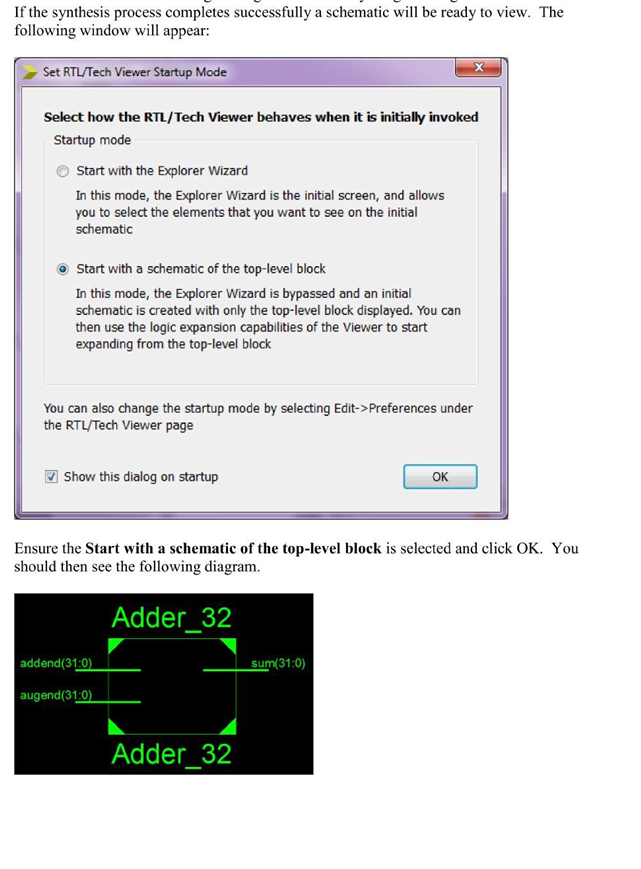
LAB 8\_ALU

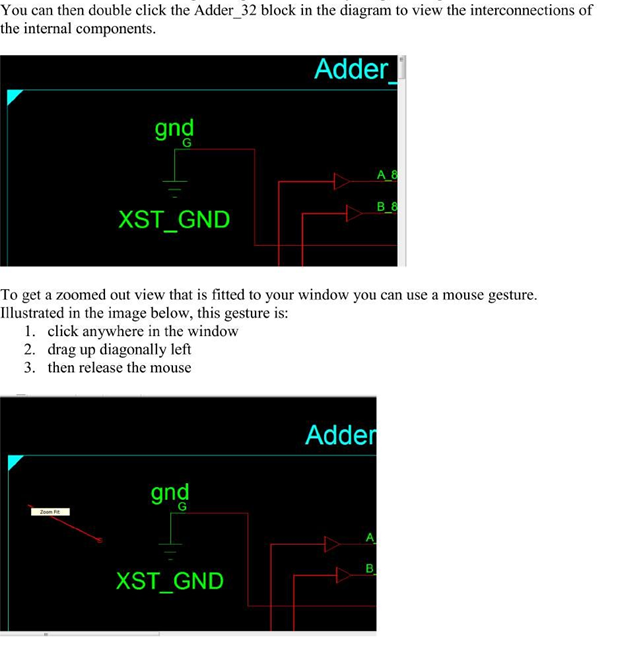




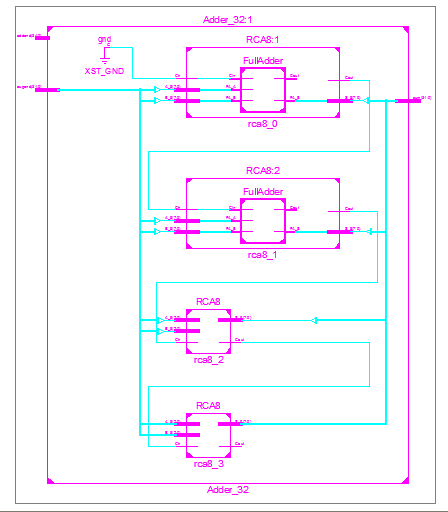
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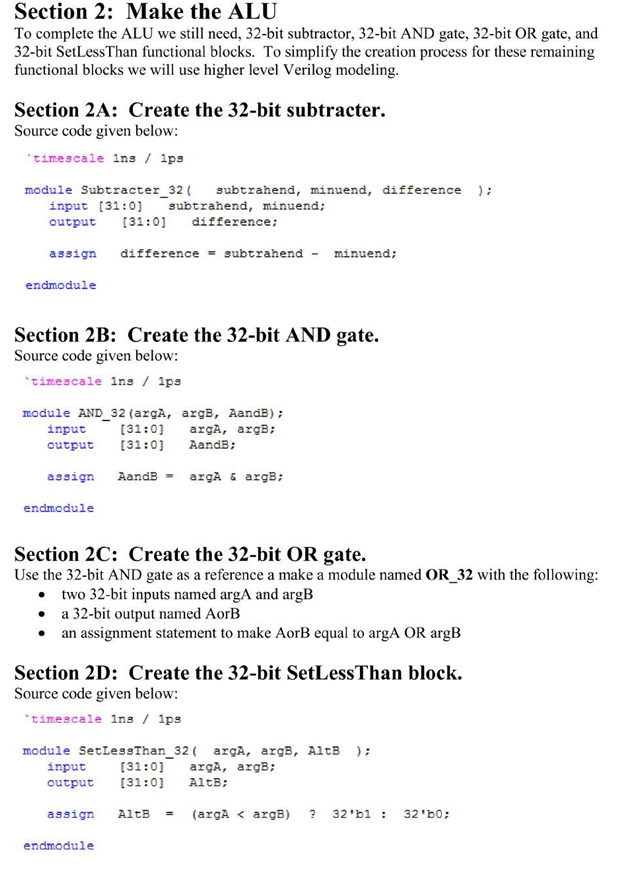
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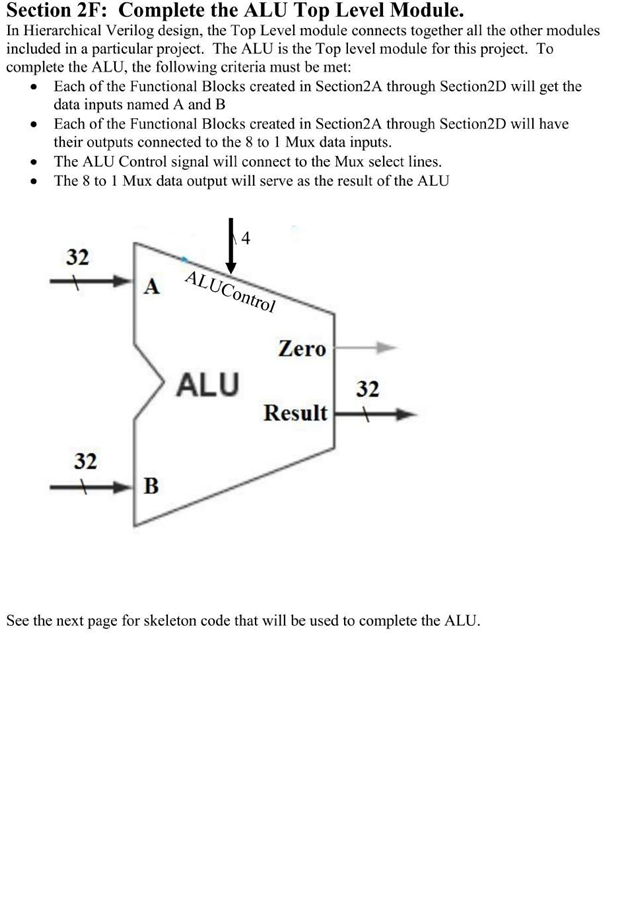
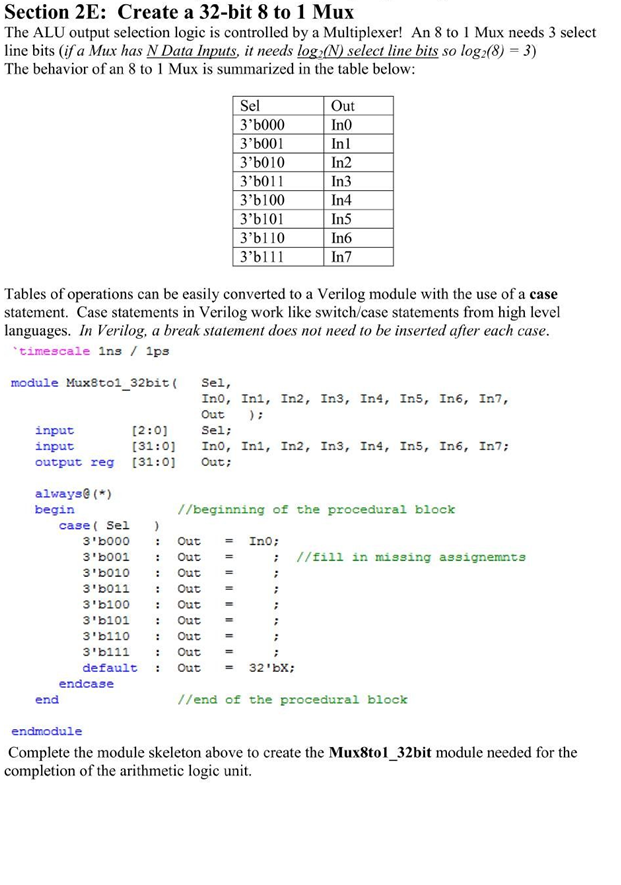
****

****

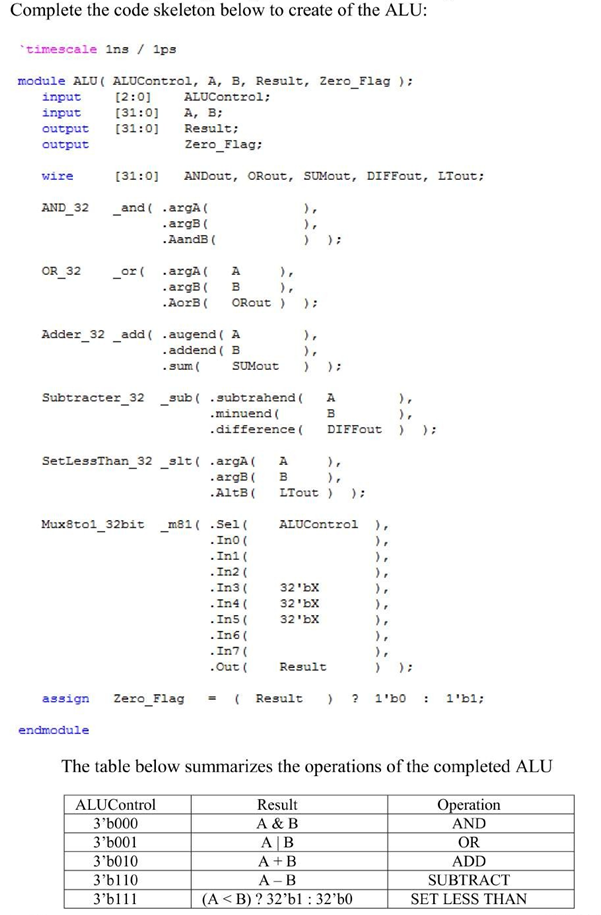
Take a screenshot of your Adder\_32 block diagram to be included with your Lab 8 report. If your Adder\_32 is built correctly, it will look identical to one on the next page:

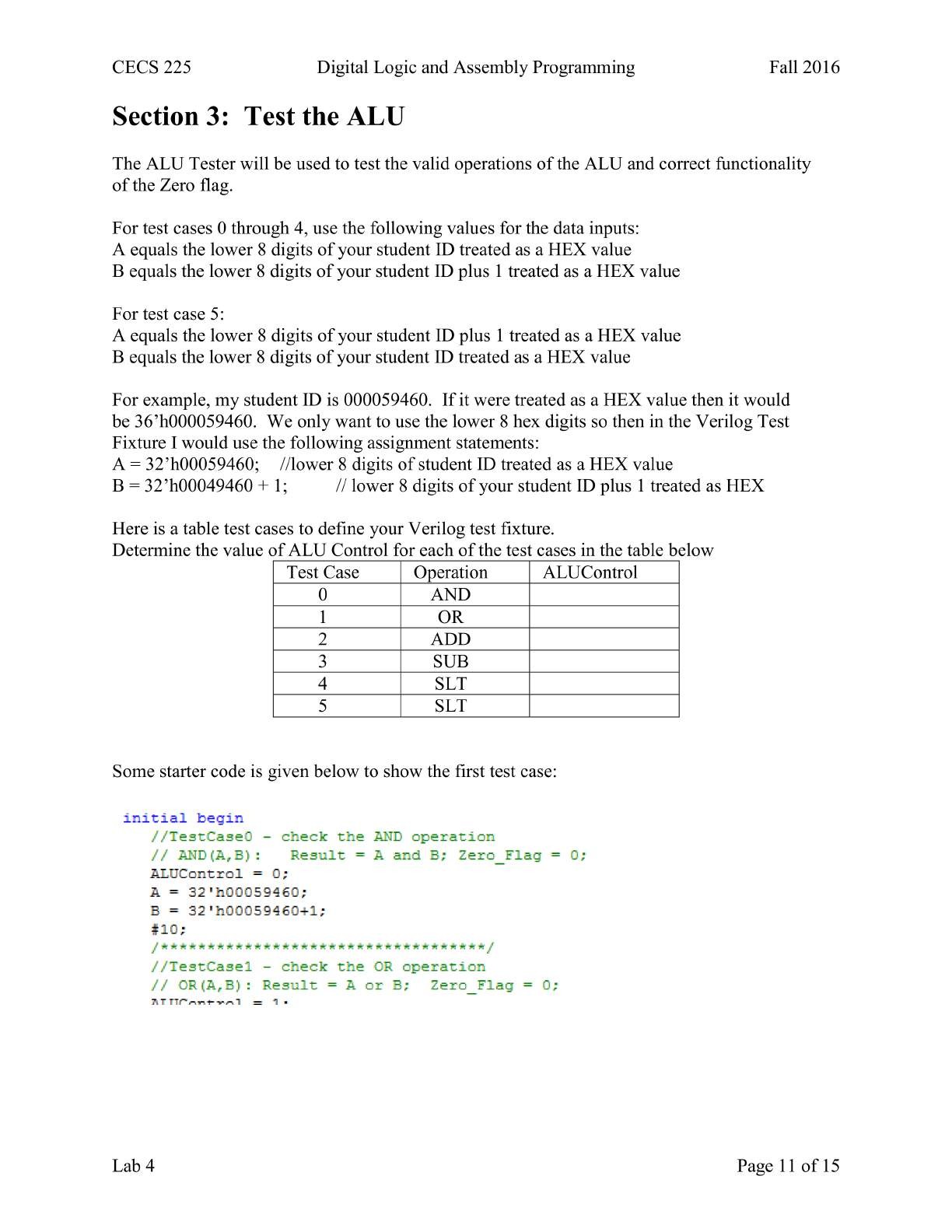






Notes: the size of the ALUControl in above figure should be 3 instead of 4!





**Format test cases with comments as shown:**

//Test case – operation to check

// Op(A,B): Result = A op B; Zero = predicted value;

*Save all the Verilog Source Files in this project, they will be used in future projects.*

**Lab 8 Report:** Submit a single PDF to beachboard with the following contents.

* **Title Page**
  + CECS 225
  + Lab 8
  + Your Name
* Section 1: all Verilog module source code including adder and block diagram/2A~2F
* Section 2: ALU Verilog Test Fixture
* Section 3: Continue to finish the following table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Test Case | ALUControl | Result | Operation | A | B | Result |
| 0 | 3’b000 | A & B | AND | 00056460 | 00059461 |  |
| 1 |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |
| 4 |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |

* Section 4: Simulation Waveform Screenshot showing correct results for all five cases

**Put each section at the beginning of a new page.**